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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KENNETH L. DEVRIES, JEFFREY P. GAMBINO, STEPHEN E. LUCE, JAMES D. WARNOCK, and FRANCIS R. WHITE

Appeal 2008-1141
Application 10/709,325[1]
Technology Center 2800

Decided: January 9, 2009

Before MAHSHID D. SAADAT, ROBERT E. NAPPI, and MARC S. HOFF, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 from a Final Rejection of claims 1-10, 19, and 20.[2] We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellants' invention relates to a silicon-on-insulator (SOI) integrated circuit including a first circuit design module having a first grid and a second

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[1] Application filed April 28, 2004. The real party in interest is International Business Machines Corporation.
[2] Claims 11-18 stand withdrawn from consideration.

circuit design module having a second grid. The first and second grids are interconnected in a fabrication layer no later than a first metallization layer that accumulates a charge during a plasma process in fabrication (para. 0015).

Claims 1 and 19 are exemplary:

1. An electronic chip, comprising:
a first circuit design module having a first grid; and
a second circuit design module having a second grid,
wherein said first grid and said second grid are interconnected in a fabrication layer no later than a first metallization layer of said chip that accumulates a charge during a plasma process in a fabrication of said electronic chip, such that said first grid and said second grid do not accumulate an excessive differential voltage due to said plasma process.

19. An electronic apparatus comprising:
at least one electronic chip, comprising:
a first circuit design module having a first grid;
a second circuit design module having a second grid; and
means for electrically interconnecting said first grid and said second grid no later than a first metallization layer that accumulates a charge during a plasma process in a fabrication of said chip.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Lui	6,869,844 B1	Mar. 22, 2005
Finzi	6,329,691 B1	Dec. 11, 2001
Kimura	3,815,771 B2	Nov. 9, 2004

Claim 19 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Liu.

Claims 1-6 and 8-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu in view of Finzi.

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu in view of Kimura.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu in view of Finzi and Kimura.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Appeal Brief (filed December 26, 2006), the Reply Brief (filed July 5, 2007), and the Examiner's Answer (mailed May 4, 2007) for their respective details.

ISSUE

The principal issue in the appeal before us is whether the Examiner erred in finding that Liu, either alone or in combination with Finzi or Kimura, teaches interconnecting a first circuit design module having a first grid and a second circuit design module having a second grid.

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

The Invention

1. According to Appellants, the invention concerns a silicon-on-insulator (SOI) integrated circuit including a first circuit design module having a first grid and a second circuit design module having a second grid. The first and second grids are interconnected in a fabrication layer no later

than a first metallization layer that accumulates a charge during a plasma process in fabrication (para. 0015).

2. Appellants define "grid" as "an interconnection between a number of points in the design module" (para. 0064).

3. In Appellants' Invention, "relatively large" metal grids are interconnected so that large charge differentials cannot build up between grid sections during plasma processing. Appellants describe "relatively large" as meaning "typically ground grids and power grids," but also including "any metallization layer having a relatively large surface area because of the large number of points interconnected" (para. 0062).

4. Appellants' Figure 3 illustrates a plurality of design modules 301-307, each of which is illustrated as a two-dimensional portion of integrated circuit chip 300.

Liu

5. Liu teaches protecting memory cells from damage induced during device fabrication by providing a protective semiconductor structure for limiting and dissipating accumulated charge from the conductive interconnects in an NROM memory array (col. 2, ll. 3-9).

6. Liu teaches a protective circuit 20, which connects word line 13 to the device substrate when charge on word line 13 becomes excessive (col. 3, ll. 26-33)

Finzi

7. Finzi teaches protecting insulated-gate semiconductor devices by providing a protective circuit including a first and second diodes connected in series between the gate and body terminals of the MOS device to be protected (col. 3, ll. 38-51).

Kimura

8. Kimura teaches layout methods for silicon on insulator (SOI) semiconductor devices (col. 1, ll. 11-14).

Dictionary definition of "grid"

9. Grid (n.)

1. a grating of crossed bars; gridiron.
2. Electricity. a. a metallic framework employed in a storage cell or battery for conducting the electric current and supporting the active material. b. a system of electrical distribution serving a large area, esp. by means of high-tension lines.
3. Electronics. an electrode in a vacuum tube, usually consisting of parallel wires, a coil of wire, or a screen, for controlling the flow of electrons between the other electrodes.
4. Surveying. a basic system of reference lines for a region, consisting of straight lines intersecting at right angles.
5. a network of horizontal and perpendicular lines, uniformly spaced, for locating points on a map, chart, or aerial photograph by means of a system of coordinates.

grid. Dictionary.com. *Dictionary.com Unabridged (v 1.1)*. Random House, Inc. http://dictionary.reference.com/browse/grid (accessed: November 10, 2008).

PRINCIPLES OF LAW

Anticipation is established when a single prior art reference discloses expressly or under the principles of inherency each and every limitation of the claimed invention. *Atlas Powder Co. v. IRECO Inc.*, 190 F.3d 1342, 1347 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79 (Fed. Cir. 1994).

Analysis of whether a claim is patentable over the prior art under 35 U.S.C. § 102 begins with a determination of the scope of the claim. We determine the scope of the claims in patent applications not solely on the

basis of the claim language, but upon giving claims their broadest reasonable construction in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). The properly interpreted claim must then be compared with the prior art.

In an appeal from a rejection for anticipation, the Appellants must explain which limitations are not found in the reference. *See Gechter v. Davidson*, 116 F.3d 1454, 1460 (Fed. Cir. 1997) ("[W]e expect that the Board's anticipation analysis be conducted on a limitation by limitation basis, with specific fact findings for each *contested* limitation and satisfactory explanations for such findings.")(emphasis added). *See also In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1734 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). *See*

also KSR, 127 S.Ct. at 1734 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.")

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *id.* at 1739, and discussed circumstances in which a patent might be determined to be obvious. In particular, the Supreme Court emphasized that "the principles laid down in *Graham* reaffirmed the 'functional approach' of *Hotchkiss*, 11 How. 248." *KSR,* 127 S.Ct. at 1739 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966) (emphasis added)), and reaffirmed principles based on its precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* The Court explained:

> When a work is available in one form of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

Id. at 1740. The operative question in this "functional approach" is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.*

Our reviewing court states that "claims must be interpreted as broadly as their terms reasonably allow." *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989). Our reviewing court further states that "the words of a claim 'are

generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc)(internal citations omitted). The "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1313. The description in the specification can limit the apparent breadth of a claim in two instances: (1) where the specification reveals a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess; and (2), where the specification reveals an intentional disclaimer, or disavowal, of claim scope by the inventor. *Id.* at 1316.

ANALYSIS

Independent claims 1 and 19, the only independent claims in the application, both require the interconnection of "a first circuit design module having a first grid" and "a second circuit design module having a second grid."

Appellants' Specification defines a "grid" as "an interconnection between a number of points in [a] design module" (FF 2). Appellants disclose that the grids that are of particular interest with respect to the invention are "sufficiently large grids," which are typically ground grids and power grids, but may also be "any metallization layer having a relatively large surface area because of the large number of points interconnected" (FF 3). Appellants' Figure 3 illustrates a plurality of design modules 301-307, each of which is illustrated as a two-dimensional portion of integrated circuit chip 300 (FF 4). Appellants' disclosures, taken together with the dictionary

definition of "grid" as "a grating of crossed bars" or "a network of horizontal and perpendicular lines, uniformly spaced, for locating points on a map" (FF 9), make it clear that a "grid" is to be construed as a "sufficiently large" two-dimensional surface area on an integrated circuit chip.

According to the Examiner, "the instant invention discloses that a grid is merely a metal line" (Ans. 11). The Examiner cites no support for this assertion, however, and we can find none in Appellants' Specification.

The Examiner's rejections of claims 1 and 19 rely on two distinct interpretations of Liu. First, the Response to Argument section of the Answer sets forth the interpretation that "a line formed between the gate electrode and a word line 13 in Figure 2 of Liu is a grid" (Ans. 11). Second, the body of the Examiner's rejection states that circuitry 12 and circuitry 14 of Liu correspond to the claimed first and second grids (Ans. 3). These two elements are interconnected, in the Examiner's view, by protective circuit 20 (*Id.*).

Because we construe "grid" as being limited to a "sufficiently large" two-dimensional surface area, and because there is no support for the Examiner's position that a grid can be a metal line, we find that, under the Examiner's first interpretation, Liu does not teach the claimed interconnection of first and second grids. Because the protective circuit 20 of Liu merely connects word line 13 to the device substrate when charge on word line 13 becomes excessive (FF 6), we find that, even under the Examiner's second interpretation, Liu fails to teach the interconnection of first and second grids.

As a result, we find error in the Examiner's rejection of claim 19 under 35 U.S.C. § 102. We also find error in the Examiner's rejection of claim 20, dependent from claim 19, under 35 U.S.C. § 103.

With respect to claim 1, we have reviewed the cited patent to Finzi and find that it does not supply a teaching of interconnecting a first grid and second grid, which we find to be absent from Liu, *supra*. Because neither Liu nor Finzi teaches interconnecting a first grid and a second grid, we find error in the Examiner's rejection of claims 1-6 and 8-10 under 35 U.S.C. § 103. We have also reviewed the cited patent to Kimura and find that it does not supply the teaching of interconnecting a first grid and second grid which we find to be absent from Liu, *supra*. Accordingly, we find error in the Examiner's rejection of claim 1, as well as claims 2-10 dependent therefrom, under 35 U.S.C. § 103.

CONCLUSION OF LAW

The Examiner erred in finding that Liu, whether alone or in combination with Finzi or Kimura, teaches interconnecting a first circuit design module having a first grid and a second circuit design module having a second grid.

ORDER

The Examiner's rejection of claims 1-10, 19, and 20 is reversed.

REVERSED

gvw

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